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A new era of crystallization: advances in polysilicon crystallization and crystal engineering

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Abstract

High-quality poly-Si microstructure is needed for the fabrication of high-quality poly-Si TFTs. The crystallization process is a very critical step of the thin film transistor (TFT) fabrication process, as it needs to satisfy conflicting requirements on material quality and cost and, at the same time, comply with the thermal-budget constraints imposed by the display substrate. Historically, solid-phase-crystallization (SPC) was the first technology to produce poly-Si films for display applications, followed by the development of laser-annealing crystallization (LAC). Both of the technologies evolved significantly over the past 20 years with a variety of spin-offs that aimed at improving different features of the poly-Si crystallization process and/or the poly-Si microstructure. This paper discusses the motivation behind the evolution process in the crystallization technology. We discuss in detail the different aspects of various crystallization techniques and provide the rationale behind our belief that lateral-crystallization technology possesses the best collection of features to enable the formation of very high-quality poly-Si films compatible with the fabrication of state-of-the-art, ultra-high performance poly-Si TFT devices.

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1. Introduction

Polysilicon thin-film-transistors (TFT) are key building blocks for active-matrix-driven flat panel displays (FPDs). Many studies have demonstrated the ability of poly-Si-based transistors to support a variety of functions beyond pixel switching, which has been the traditional role of TFTs in FPD applications. Poly-Si material enables the design of smaller TFTs that offer higher current and faster switching characteristics. As a result, pixel-driving circuits can be monolithically integrated on the display substrate.

Such integration not only reduces the amount of external interconnections to the panel, but also improves the form-factor of the resulting display. The improved performance of poly-Si TFTs is further expected to yield even deeper levels of component integration that will enable the fabrication of unique display systems. In other words, adoption of poly-Si material and technology could mark a paradigm shift in the display industry from commodity products to value-added display systems.

The fabrication of poly-Si TFTs bears many similarities to MOSFET process flow. One fundamental difference, however, exists with regards to the maximum processing temperature allowable during fabrication. Whereas the melting point of Si is the

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approximate upper limit in MOSFETs, the temperature in poly-Si TFT fabrication is typically constrained to less than 600–650 °C, due to the heat-sensitive nature of commercially available, display-grade, glass substrates. This temperature constraint has significant implications on the quality of the device active layer (poly-Si layer). The quality of a poly-Si film can be generically described as a function of the poly-Si grain size, the defect density (both within grains and at grain boundaries) and the uniformity of the microstructure over a large area. Such attributes are strongly affected by the process by which the poly-Si layer is formed (crystallization process). In addition, the complexity of the crystallization process relates directly to its cost (simpler processes being the most desirable).

High-quality poly-Si microstructure is needed for the fabrication of high-quality poly-Si TFTs. The crystallization process is a very critical step of the TFT fabrication process, as it needs to satisfy conflicting requirements on material quality and cost and, at the same time, comply with the thermal-budget constraints imposed by the display substrate. Historically, solid-phase-crystallization (SPC) was the first technology to produce poly-Si films for display applications, followed by the development of laser-annealing crystallization (LAC) [1]. Both of the technologies evolved significantly over the past 20 years with a variety of spin-offs that aimed at improving different features of the poly-Si crystallization process and/or the poly-Si microstructure. This paper discusses the motivation behind the evolution process in the crystallization technology. We discuss in detail the different aspects of various crystallization techniques and provide the rationale behind our belief that lateral-crystallization technology possesses the best collection of features to enable the formation of very high-quality poly-Si films compatible with the fabrication of state-of-the-art, ultra-high performance poly-Si TFT devices.

2. The evolution in poly-Si crystallization technology

Within the context of poly-Si TFT technology, “crystallization” refers to the step (or steps, if more than one) that are required to prepare the poly-Si material, which will be used as the TFT active layer

in the final device, from the as-deposited, thin-Si film. In the next sections we will be discussing the main features, advantages and disadvantages of two crystallization technology families, namely, SPC and LAC. State-of-the-art spin-offs include the so-called metal-induced-lateral-crystallization (MILC) technology (of the SPC family) and lateral-laser crystallization technology (of the LAC family).

2.1. Solid-phase-crystallization (SPC)

The most direct method of obtaining poly-Si films, from initially amorphous precursor-Si films, is via SPC in a furnace environment. Amorphous silicon is a thermodynamically metastable phase, possessing a driving force for transformation to polycrystalline phase given sufficient energy to overcome the initial energy barrier. SPC can be accomplished within a wide annealing temperature range that requires a similarly wide range of annealing times (i.e. time required for complete transformation of the precursor-Si film to poly-Si). The relationship between annealing temperature and annealing time, however, is not unique. In other words, depending upon the microstructural details of the precursor-Si film, different annealing times have been observed at the same annealing temperature [2]. A key factor, affecting crystallization, is the nucleation rate in the precursor-Si film. The nucleation rate is strongly influenced by the selected deposition method and conditions [3,4]. The structural order/disorder in the precursor film affects the ability of the film to form supercritical nuclei (i.e. stable nuclei), when subjected to thermal annealing. The structural order is, in turn, affected by deposition parameters such as temperature and deposition rate [3,5]. As the temperature decreases and the deposition rate increases, films are formed having a higher degree of structural disorder (thus, more difficult to nucleate).

Based on the above transformation scenario, larger grain size relates to longer crystallization time and vice versa. For practical applications, the crystallization time corresponding to average grain size exceeding 0.5–1.0 μm may be prohibitively long. The typical SPC poly-Si microstructure is characterized by a large density of structural defects (typically twin-boundaries and intra-grain microtwin defects). The result of this high grain-defect density is a saturation in the

electrical performance of poly-Si TFTs, fabricated with such poly-Si films, with grain size larger than approximately 0.3–0.5 μm . Therefore, standard SPC technology can only produce poly-Si TFTs of mediocre performance. This translates to a mobility range of 20–40 cm^2/Vs and a threshold voltage range of 3–6 V. Despite of the mediocre performance, SPC crystallization technology does offer a significant advantage in uniformity. Excellent mobility and threshold voltage uniformity has been reported for TFTs fabricated with poly-Si films crystallized by rapid-thermal-annealing. This means that SPC process may be well suited to display applications that require intermediate-level, but highly repeatable, poly-Si TFT characteristics (i.e. AM-OLEDs).

An improvement in both the SPC poly-Si microstructure, and the temperature–time parameters of the phase-transformation process can be obtained by employing SPC process in the presence of a metal catalyst [6]. In that case, the enhancement in the grain growth is attributed to an interaction of the free electrons of the metal with covalent Si bonds at the growing interface [7]. The growth enhancement has been reported for both elemental metals and metallic silicides. The nickel silicide system has received considerable attention for this application, presumably due to the very close lattice parameter match of the cubic crystal disilicide structure to c-Si (Δ of -0.4%). As a result of the growth mechanism, silicide-mediated poly-Si films demonstrate a fibrous microstructure, with each fiber attributed to c-Si growth from an individual disilicide precipitate [8]. In addition to Ni, other metals have been investigated as far as their effectiveness in enhancing Si crystal growth. These include Au, Al, Sb and In, which form eutectics with Si or Pd and Ti which form silicides with Si [9–11]. However, in all of these cases several issues were reported pertaining to the actual enhancement of the growth rate at sufficiently low crystallization temperatures (i.e. 500–550 $^{\circ}\text{C}$), and the incorporation of metal impurities in the TFT active layer. As a result, today Ni remains the undisputed metal of choice for silicide assisted crystallization. It should be noted that traces of NiSi_2 also remain within the c-Si material that is left behind, after the growth phase. This would have presented an insurmountable obstacle, had it not been for the existence of efficient gettering process [12]. This process utilizes implantation of phosphorous,

followed by low temperature annealing (at $T < 550\text{ }^{\circ}\text{C}$) to generate electrically inactive compounds. Previous studies have demonstrated the effectiveness of the gettering process in removing the remaining silicide in the film after Si crystallization [13]. The quality of crystal regions that are laterally grown by this method varies, depending upon the crystallization temperature, the crystallization time, the amount of introduced Ni metal and the extent of lateral growth. In recent years, another variation to MIC process has been proposed, to boost the Si crystal growth rate and allow the additional reduction of the crystallization temperature [14]. In this case an electric field, superimposed on the sample during MIC process, was found to enable reduction of the crystallization temperature to as low as 380 $^{\circ}\text{C}$. Different models have been invoked to explain the increase in the crystal growth rate under the applied electric field [15].

Fig. 1 shows a plot of the crystallization time versus crystallization temperature, as a function of various types of SPC technology. The mobility of the resulting poly-Si TFTs is also shown on the plot. These data illustrate that the advances in SPC, made possible by the enhanced crystal growth, due to trace amount metals in silicon, has enabled a tremendous improvement in poly-Si TFT performance, as well as a reduction in the crystallization temperature–time requirements. Mobility values in the order of $\sim 100\text{ cm}^2/\text{Vs}$ are sufficient to enable partial integration of driving circuits on the display substrate. However, additional improvements in performance are required to increase the level of on-panel integration and enable the fabrication of advanced display systems. Laser-annealing has been investigated as an alternative crystallization technology with the potential of meeting such performance demands.

2.2. Excimer laser crystallization (ELC) technology

Typical excimer lasers operate in pulse mode, at frequencies around 300 Hz, with pulse duration in the range of 10–50 ns. The energy output of TFT production excimer lasers (i.e. Lambda Physik STEEL series) is in the order of 0.6–2 J [16]. It should be noted that very powerful XeCl excimer lasers, developed by the European maker SOPRA, have also been applied to poly-Si annealing [17]. In that case, the energy of the laser is $\sim 15\text{ J}$, the pulse

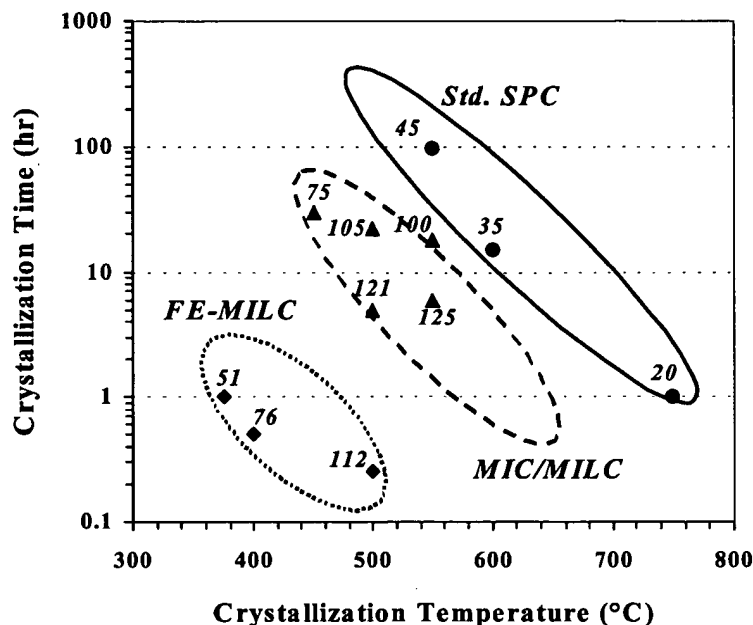


Fig. 1. Plot of the crystallization time vs. crystallization temperature, as a function of the type of SPC technology. The numbers, within the plot area, denote the mobility of poly-Si TFTs made by the relevant SPC technology. SPC, solid-phase-crystallization; MIC, metal-induced crystallization; MILC, metal-induced-lateral-crystallization; FE-MILC, field-enhanced MILC.

duration ~ 220 ns and the discharge frequency ~ 1 –5 Hz. It is now well understood that the pulse-to-pulse repeatability of the excimer laser is the most important attribute of the laser equipment, followed by the discharge frequency, output energy and pulse duration. It is convenient to use a simple classification scheme to understand the impact of each laser parameter to (a) productivity and (b) film quality. In that sense, pulse-to-pulse repeatability, discharge frequency and output energy affect primarily productivity, whereas pulse duration affects primarily the film quality. As productivity tends to be the number one priority in manufacturing operations, laser equipment featuring excellent repeatability and high discharge frequency (with reasonable output energy) are preferable. The pulse-to-pulse repeatability of state-of-the-art laser equipment configured for Si annealing application is currently in 6–9% 3σ range. This number is expected to decline further to $\sim 4\%$ within 3 years. Analysis of the transformation scenarios associated with ELC, show that one can categorize ELC of Si films in terms of three transformation regimes (occurring at low, intermediate and high laser fluence, respectively) [18,19].

The low laser fluence regime describes a situation where the incident laser fluence is sufficient to induce melting of the Si film, but it is low enough that a continuous layer of Si remains at the maximum extent of melting. For this reason, this regime is also referred to as “partial-melting” regime. For irradiation of a-Si films, this regime is characterized by a combination of explosive crystallization and vertical solidification. Explosive crystallization can be triggered at the onset, or near the end of melting, respectively, depending upon the presence or absence of microcrystallites in the Si film [20].

The high laser fluence regime corresponds to the situation encountered when the laser fluence is sufficiently high to completely melt the Si film. For this reason, this regime is also referred to as “complete-melting” regime. The mechanism of transformation in this regime relates to the nucleation of solids within the liquid for the formation of a stable solid-liquid interface that can be used to “accommodate” the liquid-to-solid conversion. The nucleation in this case takes place as a result of the unusually deep undercooling that occurs in the molten-Si film. The term “undercooling” refers to the degree of deviation of the

temperature of the molten-Si from its melting point. In that sense, deep undercooling implies a liquid existing at a temperature substantially lower than its melting point. As a result of the copious nucleation that occurs within the undercooled molten-Si, the grain sizes obtained in this regime are very small (typically in the order of tens of nanometer in diameter).

In addition to these two regimes, a third regime has been found to exist, within a very narrow experimental window, in-between the two main regimes (superlateral-growth region, SLG). Despite of the small extent of this third region, it is nonetheless one of great technological significance, as the poly-Si films formed within this region feature large-grained polycrystalline microstructures (i.e. grain sizes of several multiples of the film thickness). The transformation scenario associated with this regime has been modeled by Im and others, in terms of near-complete-melting of Si films [18,21]. Particularly, it was argued that at the maximum extent of melting, the unmelted portion of the underlying Si film no longer forms a continuous layer, but instead consists of discrete islands of solid material separated by small regions that have undergone complete-melting. For this reason, this regime is referred to as the “near-complete-melting” regime. The practical implication of this model is that the unmelted islands provide solidification “seeds”, from which lateral growth can ensue, thus propagating the solid-liquid interface within the surrounding undercooled molten Si (for this reason this regime has been also coined as SLG regime). In the ideal case, the lateral growth fronts coalesce and form a continuous

matrix of similarly sized grains. This, however, is very difficult to control in practice as the laser fluence leading to SLG regime needs to be precisely controlled. Small variations in the laser fluence (i.e. due to pulse-to-pulse energy variations) lead to either partial- or complete-melting conditions, with grave implications to the poly-Si microstructure as discussed before. Therefore, within the SLG regime, the high-quality of the resulting poly-Si material is usually compromised by difficulties in achieving this quality uniformly, across the irradiated film. Fig. 2 shows the average grain size and corresponding poly-Si TFT performance, associated with each of these three laser crystallization regimes.

In conventional laser crystallization, the substrate is scanned under the laser beam, which is typically homogenized to a “top-hat” profile. Other beam profiles have also been employed, in efforts to improve the uniformity of the resulting microstructure [22], but the top-hat profile is generally considered as the industry standard. The aim of this process is to induce near-complete-melting in the film and, by irradiating the same region multiple times, improve the size and uniformity of the initially developed grains. This scenario has similarities to conventional normal or secondary grain-growth process and has been previously discussed in detail [23]. In practice, this scenario can be achieved either by static irradiation of a region for multiple times (before moving to the next area), or, on-the-fly, by employing a sufficiently wide overlap between successive shots. The first approach is more suited to a large-area beam, whereas the second approach is commonly used with

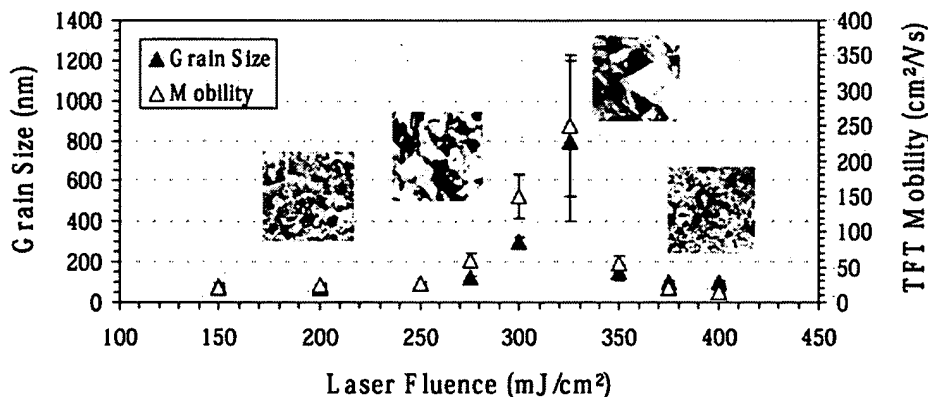


Fig. 2. Grain size and corresponding poly-Si TFT mobility vs. laser fluence for conventional ELC process. The inset TEM photographs illustrate the poly-Si microstructure corresponding to (left to right) surface-, partial-, near-complete- and complete-melting regime.

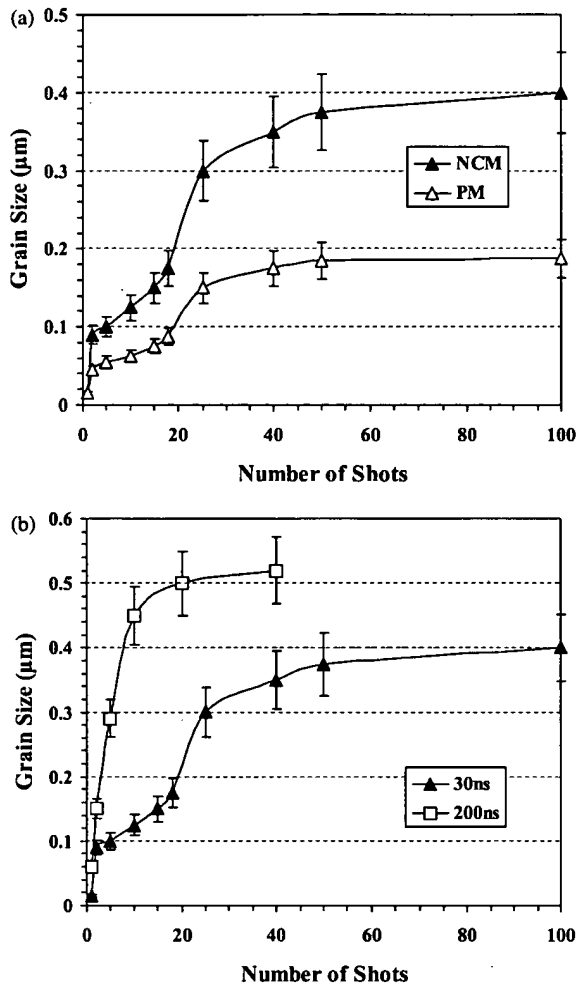


Fig. 3. (a) Poly-Si grain size vs. number of shots. NCM corresponds to irradiations at the near-complete-melting regime. PM corresponds to irradiations at the partial-melting regime. The number of shots (NS) relates to overlap (OL) by the simple relationship: $OL = (NS - 1)/NS$. (b) Poly-Si grain size vs. number of shots and laser pulse duration (all irradiations at the NCM regime).

small-area, high-aspect-ratio beams [24,25]. Naturally, a limitation exists in the practical range of the number of shots (or the overlap distance) dictated in the low end by material quality considerations and in the high end by productivity (i.e. throughput) considerations. Fig. 3(a) and (b) shows the variation of grain size with the number of shots on a given area.

Development of conventional ELC method has been able to provide poly-Si material of higher quality than conventional SPC method. This is primarily attributed

to the melt-induced poly-Si growth. As a result of such growth, substantially fewer intra-grain-defects form within the grains of laser-annealed poly-Si films. This improvement seems to be more important than the improvement in the grain size itself, as evidenced by the trend in the TFT mobility of poly-Si films as a function of grain size and annealing method (SPC or ELC) ([26], see also Fig. 4). However, the stable grain size of ELC poly-Si films is typically limited to 0.3–0.6 μm . Larger grain size is possible within the SLG window, but this regime is intrinsically unstable within the context of conventional ELC process. For conventional ELC, a laser equipment attribute that improves the grain size, within the stable regime, is pulse duration. Longer pulse duration has been found to yield larger grain size (Fig. 3(b)). Theoretical arguments, coupled with simulation results, have attributed this to an increase in the degree of undercooling in the molten-Si film that enables longer solidification time before the onset of copious nucleation.

One disadvantage of conventional ELC process relates to the difficulty in maintaining a proper balance between performance and process uniformity. This comes about because the pulse-to-pulse repeatability (which is equipment-related parameter) defines the process window that the laser fluence needs to be centered to avoid crossing over to other ELC regimes during annealing. This fluence window, in turn, defines the range of performance that can be expected from TFTs fabricated on such poly-Si microstructure. In manufacturing operations, this kind of compromise, typically, translates to only mediocre TFT performance (i.e. $100 \text{ cm}^2/\text{Vs}$) at the benefit of wider process window. A second disadvantage of conventional ELC process is the relative disparity between the average grain size and the TFT channel size (length). This means that unless the TFT channel becomes extremely small (i.e. $<0.5 \mu\text{m}$) it will be impossible to imagine the TFT channel consisting of a single grain. This problem is further exacerbated by the lack of tight grain size distribution in conventional ELC and the inability to precisely control the location of grain boundaries with respect to the TFT channel. Therefore, the application of conventional ELC process is limited due to these issues and cannot be expected to provide a technology path for future devices. However, this is not to say that laser crystallization is not capable of resolving these issues and improving device

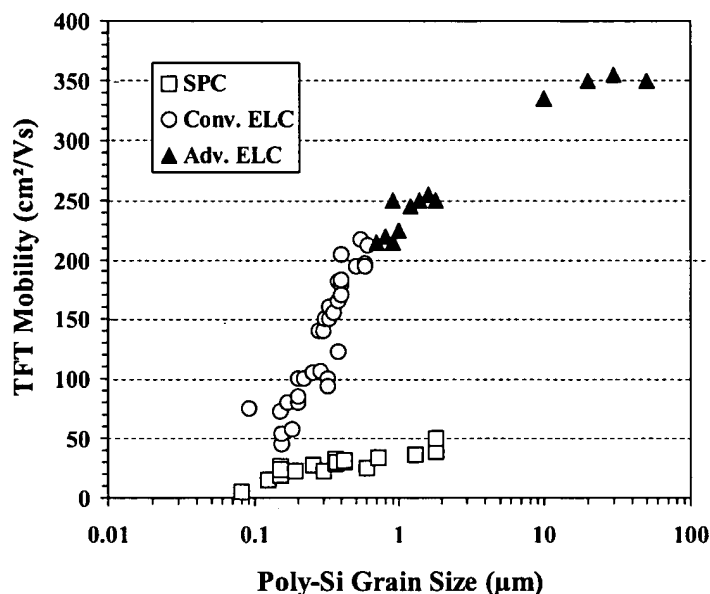


Fig. 4. TFT mobility as a function of poly-Si grain size. For a given grain size, ELC process enables superior TFT performance due to the significant reduction of defects within the poly-Si grains. Advanced ELC schemes enable customization of the crystal domain size. When the crystal domain size exceeds that of the device channel length very high mobility values can be obtained (independent upon additional increases in the domain size).

performance. By rethinking the physics of laser crystallization and cleverly exploiting previous results, a number of elegant solutions have been indeed identified and developed over the past few years, giving rise to a new generation of LAC technologies that will be discussed next.

2.3. Advanced (lateral growth) ELC technology

The key point that drives development of advanced ELC concepts is the manipulation of the intrinsically unstable SLG phenomenon in a manner that permits flexible design of the resulting material microstructure, while eliminating all the caveats that are associated with conventional ELC processing in the SLG regime [27]. In that sense, all such concepts can be classified under the general term of “controlled SLG (C-SLG)” [28].

SLG occurs as a consequence of the lowering in the free energy of the solid-Si/molten-Si system, by the growth of the former (solid-Si) into the undercooled liquid (molten-Si) region. By exploiting this concept, artificial situations can be devised that allow precisely controlled regions of the silicon film to be melted and

left in contact with solid regions. These solid regions can then act as seeds for lateral growth of material into the undercooled liquid. The most obvious advantage of C-SLG process is the relative insensitivity of this process to variations in the laser fluence. In the case of C-SLG, the requirement is that the laser fluence is at least sufficient to completely melt the irradiated region, which is in contact with the solid region that will serve as the seed for lateral growth. Note that higher fluence, than this minimum requirement, will work equally well. This implies a wider process window than that of the naturally occurring SLG regime, where the objective is to leave sufficient number of isolated solid islands by precisely controlling the fluence level within the irradiated area (Fig. 5).

By controlling the shape and physical dimensions of the regions that undergo complete-melting through various optical, photolithographic and/or other means, the resulting microstructure can be tailored to yield controllable, predictable and uniform grain size and structure. This point is the direct consequence of the relationship between the lateral growth distance (extending in the direction of lateral growth) and the width of the irradiated (completely molten) region.

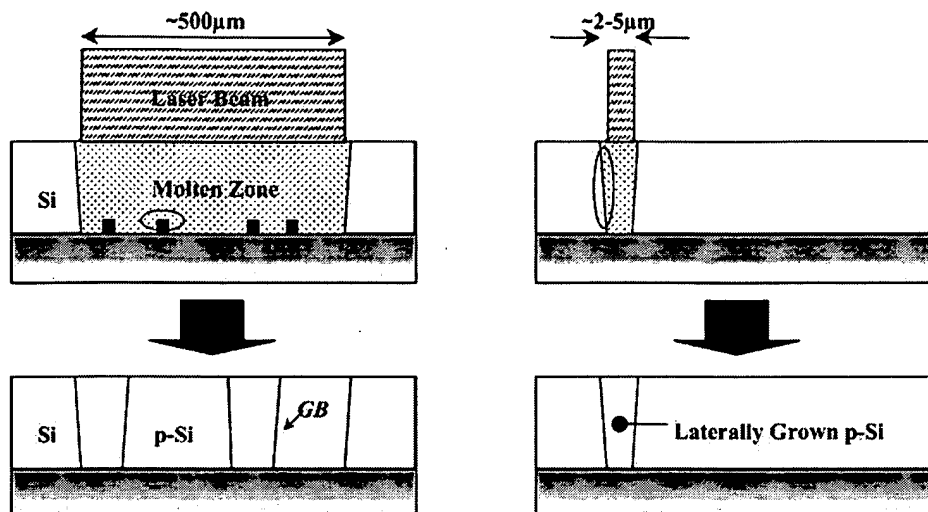


Fig. 5. Comparison of SLG and C-SLG modes of growth. In SLG (left panels) growth initiates from seeds, which survived the melting process, at the Si-SiO₂ interface. In C-SLG (right panels) the poly-Si microstructure forms by lateral epitaxy from seeds generated at the liquid-solid interface. Notice the difference in the width of the molten zone between SLG and C-SLG.

The growth distance of the lateral-crystals is limited either by the onset of nucleation in the molten zone, or by collision with the lateral grown crystals from the opposite side of the molten region. Therefore, by tailoring the width of the molten region that is formed during the laser irradiation to the lateral growth distance, the copious nucleation can be avoided. In this manner, a very uniform and large-grained microstructure can be generated over large areas.

Several techniques can be identified to carry out the task of pre-selecting the regions to undergo complete-melting. These include varying the thickness or contour of the Si film, coating the Si film with a patterned overlayer that can act as an antireflective, reflective, beam-absorbing or heat-sink medium and shaping the intensity profile of the incident laser beam via proximity or projection irradiation involving a shadow mask, by inducing interference on the film surface, or by using diffractive phase elements [29–33]. Fig. 6 presents illustrations for a number of published lateral-ELC concepts, including projection irradiation, phase-shift masking and modification of heat diffusion pattern by overlayer/underlayer engineering [28,34,35]. In other related studies, researchers have also demonstrated the formation of high-quality, laterally-grown poly-Si films via solid-state laser irradiation in the visible range [36,37].

3. Performance of advanced ELC poly-Si TFTs

Poly-Si TFTs have been fabricated by various groups, including ours, using advanced ELC process (relying on lateral poly-Si growth). Fig. 7 summarizes *n*-channel poly-Si TFT characteristics as a function of the ELC process type. We distinguish two cases, depending upon the relationship of the crystal domain size (i.e. grain size) to the device channel length. Different ELC technologies have been mapped out with this classification scheme. It is shown that as the crystal domain size increases, and becomes equivalent to the device channel length, significant improvement in the device performance is observed. In the ideal case, SOI-level performance is sought, which seems to be successfully approximated by some of the best-performing ELC technologies on this plot. The fundamental difference between the performance level achieved by the various ELC techniques has its root in the type and density of defects present in the poly-Si active layer. Depending upon the type of lateral-ELC process, the density, type and orientation of grain boundaries, present in the TFT channel, may differ. Such parameters affect the absolute TFT performance and uniformity and present some challenges on the selection of process technology for the fabrication of poly-Si TFTs, especially as the

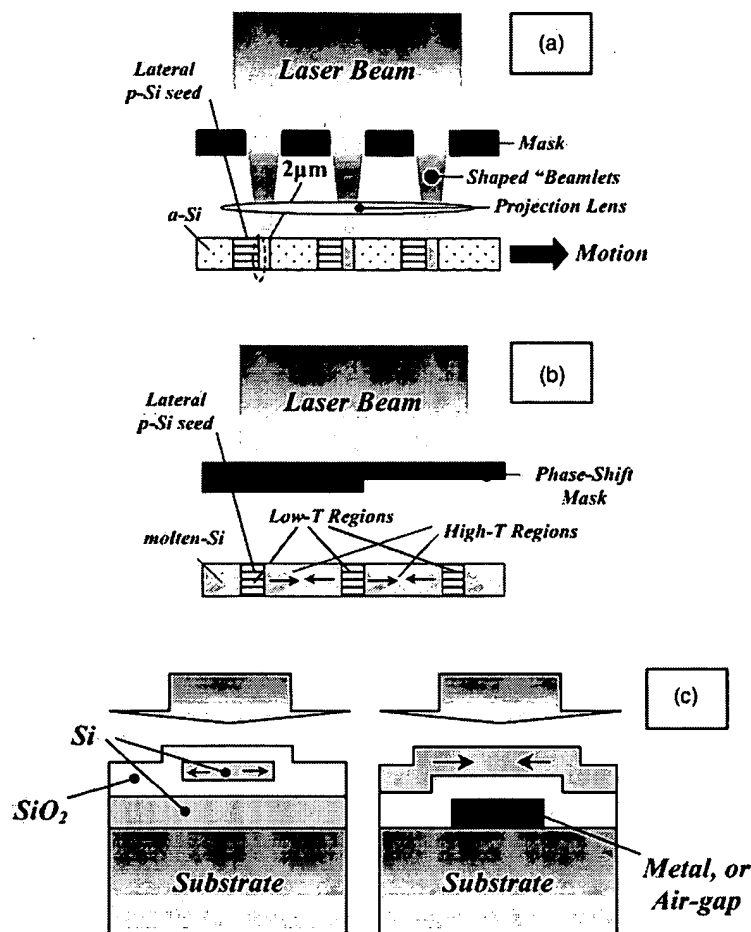


Fig. 6. Illustration of different schemes aiming to achieve controlled super-lateral growth by (a) projection irradiation of the laser beam through a mask pattern (SLS); (b) projection through phase-shift mask (PMELA); and (c) modification of heat flow through overlayer or underlayer engineering (P²-ELA, air-gap structure, etc.).

device channel length decreases. One disadvantage that is currently noted, for lateral-ELC schemes, is the existence of "directionality" in the TFT performance. In other words, TFT characteristics demonstrate a strong dependence on the degree of misorientation between the direction of carrier conduction in the active layer and the lateral growth direction in the film ([38], see also Fig. 8). Practical solutions to such problems will be also required. Despite the occurrence of such issues, however, one has to acknowledge that application of advanced, laser-based crystallization processes in TFT fabrication makes possible the improvement of both performance and uniformity of poly-Si TFTs, to levels not possible

before [34,37,39]. The powerful features of the new poly-Si materials can be clearly seen by comparing the signal propagation delay time, extracted from CMOS ring-oscillator test-circuits fabricated with various poly-Si materials (Fig. 9). The improvement in material quality, made possible by the advanced crystallization technology, enables the fabrication of smaller transistors that exhibit faster operation under a reduced driving voltage range. The reduction in the device size is made possible by the higher material performance due to the improved quality of the poly-Si active layer. The reduction in the driving voltage range is a direct consequence of the substantially lower density of trap states in the poly-Si active layer

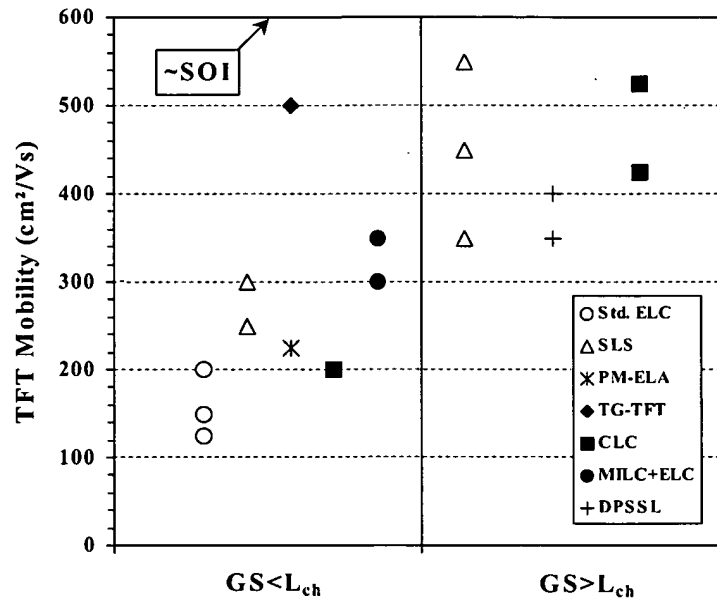


Fig. 7. Comparison of the mobility of *n*-channel poly-Si TFT prepared by different, lateral-ELC techniques (standard ELC performance is provided as a reference). The TFT mobility is also cross-referenced by the relation of the crystal domain size (i.e. grain size, GS) to the device channel length (L_{ch}). SLS, sequential lateral solidification; PM-ELA, phase-mask excimer-laser-annealing; TG-TFT, twin-grain TFT; CLC, CW-laser lateral-crystallization; MILC, metal-induced-lateral-crystallization; DPSSL, diode-pumped solid-state-laser crystallization.

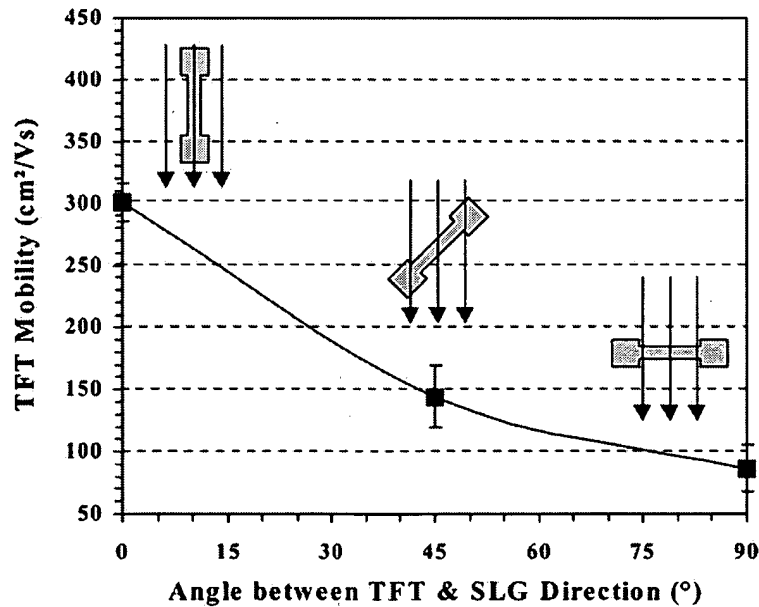


Fig. 8. Poly-Si TFT mobility as a function of the angle between the direction of the TFT channel and the direction of lateral growth (SLG direction).

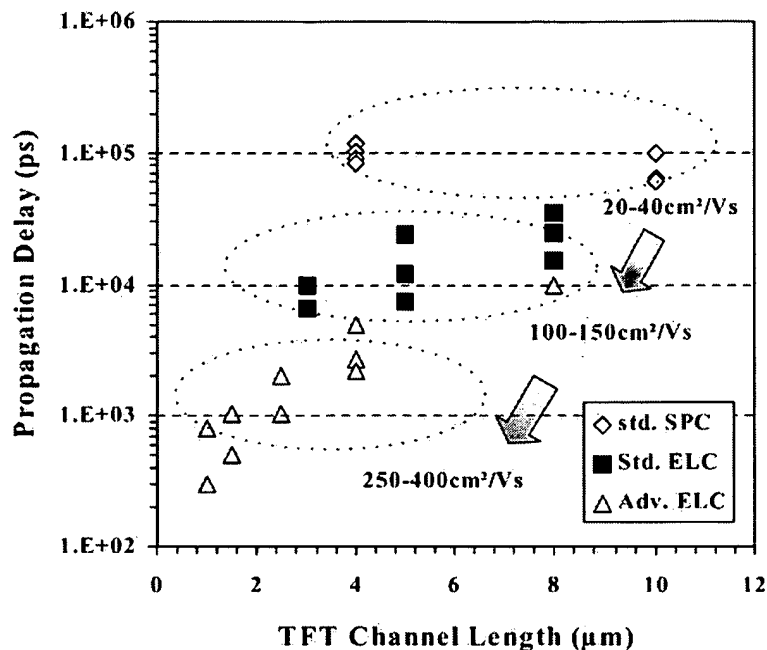


Fig. 9. Comparison of the propagation delay time, extracted from CMOS ring-oscillator test-circuits, as a function of the crystallization technology and the TFT channel length. Higher performance circuits are possible by adopting advanced ELC lateral-crystallization schemes.

that enables a decrease in the threshold voltage and an increase in the sub-threshold swing of the device. Lateral-ELC poly-Si material clearly yields a device performance level that is suitable not only for the integration of peripheral driving circuits but that of

more advanced components (i.e. amplifiers, dc/ac converters and timing controllers). Such components are expected to fulfill the vision of system-LCDs and system-on-panel concepts that have been envisioned more than a decade ago.

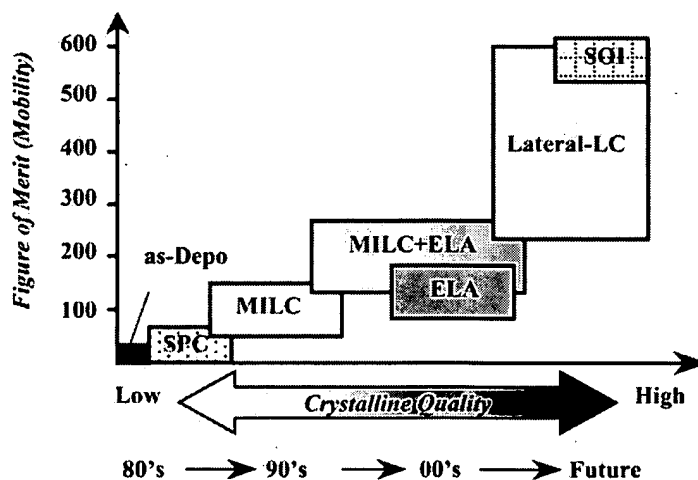


Fig. 10. Correlation between TFT mobility and poly-Si crystallization technology.

4. Summary/conclusions

Fig. 10 summarizes the typical performance data for the different crystallization technologies covered in this report. Historically, SPC has been the first method to produce poly-Si films for TFT applications. Since that time, around the early 80s, many other techniques have emerged, aiming to improve the film quality and TFT characteristics to enable new, more demanding display applications.

Metal-induced-crystallization (MIC) has provided a high-end SPC technology that has been shown capable of producing poly-Si TFTs with very high performance and uniformity, albeit the need to combine SPC and conventional ELC methods to achieve that performance level. The main caveat of SPC technology, which is intra-grain-defects, seems impossible to effectively tackle, given the temperature constraints of common display-glass substrates. Therefore, the next evolution in crystallization technology points to laser technology, in some format, as the logical choice. It is fair to state that ELC technology has significantly improved and matured, on both process and equipment technology, over the past 20 years. However, it is only within the last decade that the accumulation of experimental data and related observations has led to theoretical understanding that has made possible novel crystallization scenarios. As a result, advanced laser-annealing schemes, exploiting the SLG phenomenon, are already producing very high-quality, uniform poly-Si microstructures and are expected to produce material capable of performance rivaling that of single-crystal Si in the near future. It should be noted that, in addition to the sought high-crystal Si quality, future processing schemes need also consider alignment of such crystal “islands” with the device active region. Feasibility of such crystallization schemes has been demonstrated but, clearly, more work is needed in that area [35,40].

References

- [1] A. Mimura, N. Konishi, K. Ono, J.I. Ohwada, Y. Hosokawa, Y.A. Ono, T. Suzuki, K. Miyata, H. Kawakami, *IEEE Trans. Electron Dev.* 36 (1989) 351.
- [2] A.T. Voutsas, M.K. Hatalis, *J. Electrochem. Soc.* 139 (1992) 2659.
- [3] A.T. Voutsas, M.K. Hatalis, *J. Electrochem. Soc.* 140 (1993) 871.
- [4] A.T. Voutsas, M.K. Hatalis, *J. Electron Mater.* 23 (1994) 319.
- [5] K. Nakazawa, *J. Appl. Phys.* 63 (1991) 1703.
- [6] R.S. Wagner, W.C. Ellis, *Appl. Phys. Lett.* 4 (1964) 89.
- [7] F. Spaepen, E. Nygren, A.V. Wagner, in: *Crucial Issues in Semiconductor Materials and Processing Technologies*, NATO ASI Series E: Applied Sciences, vol. 222, Kluwer Academic Publishers, Dordrecht, 1992, p. 483.
- [8] C. Hayzelden, J.L. Batstone, *J. Appl. Phys.* 73 (1993) 8279.
- [9] L. Hultman, A. Robertsson, H.T.G. Hentzell, I. Engstrom, *J. Appl. Phys.* 62 (1987) 3647.
- [10] G. Radnoczi, A. Robertsson, H.T. Hentzell, S.F. Gong, M.A. Hasan, *J. Appl. Phys.* 69 (1991) 6394.
- [11] R.J. Nemanichi, C.C. Tsai, M.J. Thompson, T.W. Sigmon, *J. Vac. Sci. Technol.* 19 (1981) 685.
- [12] P.F. Schmidt, US Patent 4231809 (1980).
- [13] T. Takayama, H. Ohtani, A. Miyana, T. Mitsuki, H. Ohnuma, S. Kanajima, S. Yamazaki, in: *Proceedings of AMLCD'00*, 2000, p. 25.
- [14] S.J. Park, B.R. Cho, K.H. Kim, K.S. Cho, S.Y. Yoo, A.Y. Kim, J. Jang, D.H. Shin, *SID Symp. Digest XXXII* (2001) 562.
- [15] S.Y. Yoon, J.Y. Oh, C.O. Kim, J. Jang, *J. Appl. Phys.* 84 (1998) 6463.
- [16] M. Fiebig, U. Stamm, P. Oesterlin, N. Kobayashi, B. Fechner, *SPIE Proc.* 4295 (2001) 38.
- [17] C. Prat, D. Zahorski, Y. Helen, T.M. Brahim, O. Bonnaud, *SPIE Proc.* 4295 (2001) 33.
- [18] J.S. Im, H.J. Kim, M.O. Thompson, *Appl. Phys. Lett.* 63 (1993) 2969.
- [19] M.A. Crowder, Ph.D. dissertation, Columbia University, 2001.
- [20] W. Sinke, F.W. Saris, *Phys. Rev. Lett.* 53 (1984) 2121.
- [21] J.S. Im, H.J. Kim, *Appl. Phys. Lett.* 64 (1994) 2303.
- [22] S.D. Brotherton, D.J. McCulloch, M.J. Edwards, *Solid State Phenom.* 37/38 (1994) 299.
- [23] H. Kuriyama, K. Sano, S. Ichida, T. Nohda, Y. Aya, T. Kuwahara, S. Noguchi, S. Kiyama, S. Tsuda, S. Nakano, *Mater. Res. Soc. Symp. Proc.* 297 (1993) 657.
- [24] A.T. Voutsas, C. Prat, D. Zahorski, in: *Proceedings of the Conference Record on IDRC'00*, 2000, p. 451.
- [25] S.D. Brotherton, D.J. McCulloch, J.B. Clegg, J.P. Gowers, *Excimer-laser-annealed poly-Si thin-film transistors*, *IEEE Trans. Electron Dev.* 40 (1993) 407.
- [26] M.K. Hatalis, A.T. Voutsas, in: *Proceedings of the Conference on RTP'01*, 2001.
- [27] J.S. Im, R.S. Sposili, *Mar. Res. Soc. Bull.* 21 (3) (1996) 39.
- [28] J.S. Im, M.A. Crowder, R.S. Sposili, J.P. Leonard, H.J. Kim, J.H. Yoon, V.V. Gupta, H.J. Song, H.S. Cho, *Phys. Stat. Sol. A* 166 (1998) 603.
- [29] K. Makihiro, T. Asano, in: *Proceedings of AMLCD'00*, 2000, p. 33.
- [30] H.J. Kim, J.S. Im, *Appl. Phys. Lett.* 68 (1996) 1513.

- [31] P. van der Wilt, R. Ishihara, J. Bertens, *Mater. Res. Soc. Symp. Proc.* 621 (2000) Q7.4.1.
- [32] R.S. Sposili, J.S. Im, *Appl. Phys. Lett.* 69 (1996) 2864.
- [33] M. Matsumura, *SPIE Proc.* 4295 (2001) 1.
- [34] C.-H. Kim, I.-H. Song, W.-J. Nam, M.-K. Han, *IEEE Electron Dev. Lett.* 23 (2002) 315.
- [35] M. Matsumura, in: *Proceedings of IDRC'99*, 1999, p. 351.
- [36] Y. Helen, R. Dassow, M. Nerding, K. Mourgues, F. Raoult, J.R. Köhler, T. Mohammed-Brahim, R. Rogel, O. Bonnaud, J.H. Werner, H.P. Strunk, *Thin Solid Films* 383 (2001) 143–146.
- [37] N. Sasaki, A. Hara, F. Takeuchi, Y. Mishima, T. Kakehi, K. Yoshino, M. Takei, *SID Symp. Digest* 33 (2002) 154.
- [38] Y.H. Jung, J.M. Yoon, M.S. Yang, W.K. Park, H.S. Soh, H.S. Cho, A.B. Limanov, J.S. Im, *Mater. Res. Soc. Symp. Proc.* 621 (2000) Q8.3.1.
- [39] S.D. Brotherton, M.A. Crowder, A.B. Limanov, B. Turk, J.S. Im, in: *Proceedings of the Conference Record of ICDR'01*, 2001, p. 387.
- [40] P. van der Wilt, B.D. van Dijk, G.J. Bertens, R. Ichihara, *Mater. Res. Soc. Symp. Proc.* 685E (2001) D5.20.1.